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(54) Memory unit comprising a memory and a protection unit

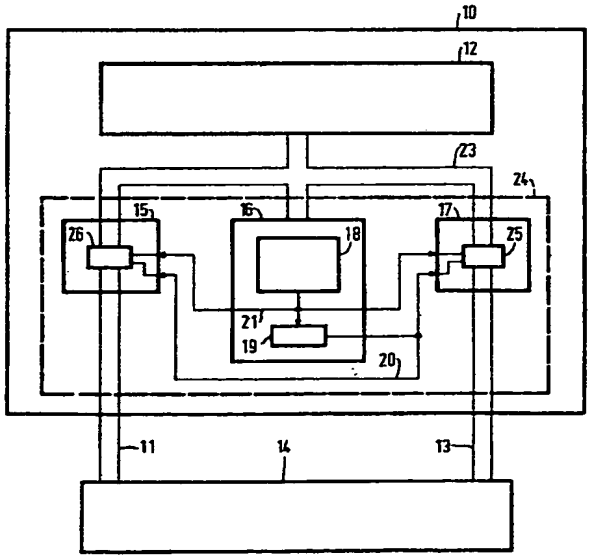
(57) A memory unit in which preselected program words stored in some of the memory locations are modified before transmission to the output pins of the memory unit, in order to protect those program words against illegal copying.

When a jump instruction is decoded, the decoder issues a command to a random number generator 19, to an adder 25 and to a subtractor 26. The adder adds the random number output by the generator to the destination address of the pump instruction to form a pseudo-jump address which is sent to the processor 14.

When the processor subsequently addresses the memory 12 to acquire the program word, the pseudo-jump address is converted to the original destination address by the subtractor.

Copying pseudo-addresses results in the copied program being useless.

Address tables may be used instead of the random number generator, adder and substractor.



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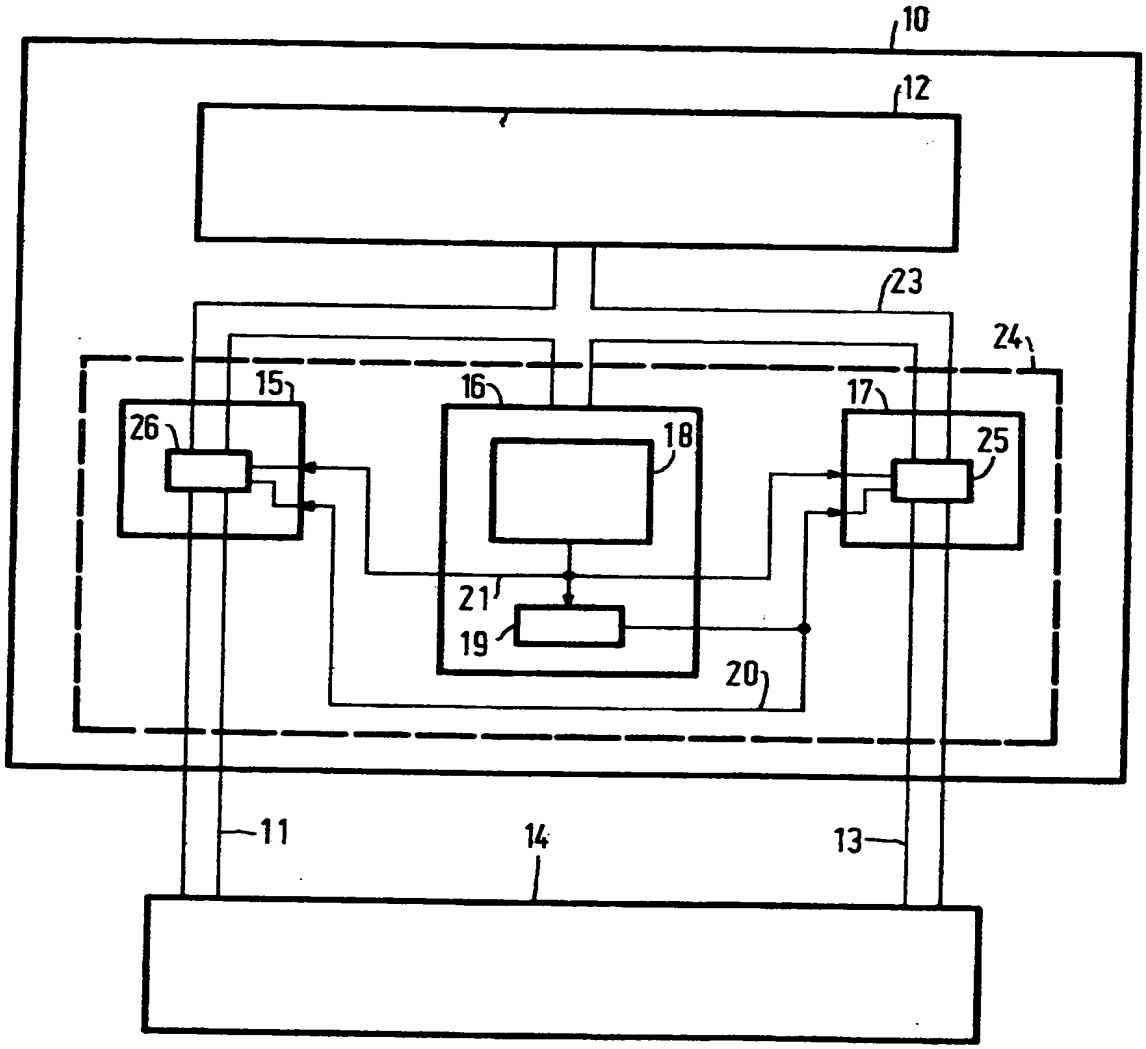

SPECIFICATION

Memory unit comprising a memory and a protection unit

The invention relates to a data processing system comprising a data processor and a memory unit which comprises a protection unit and a memory for the storage of at least one program comprising a plurality of program words, said memory having a port for the exchange of information words, each information word comprises a program word and his respective address word, said protection unit comprises:

– recognition means having first input connected to said port and being provided for recognition out of the flux of information words at said port those which belong to a predetermined group wherein the information words have a program word which comprises an address part for addressing a further program word, said recognition means being further provided for generating a command signal thereupon;

– first modification means, having a second input connected to said port and a third input connected to said recognition means for receiving said command signal, said first modification means being provided for applying under control of said command signal a first modification operation on a received program word, said first modification means being connected to a first data output of said memory unit;

said data processor comprises:

– a data input connected to said first data output for receiving data signals;

- a program counter which is settable under control of received data signals;

– a first address output connected to a first address input of the memory unit for supplying address signals in a sequence determined by said program counter.

Such a data processing system being described in the Dutch patent application nr. 82 01 847 laid open to public inspection on 01-12-'83. The memory unit comprises a protection unit for protecting the program words stored in the memory against illegal copying by unauthorized copiers.

Devices which are controlled by a date processor unit comprise a memory, for example, a ROM or a PROM, in which programs and other information (termed software), are stored in the form of program words for the execution of data processor operations. The design of such software is time consuming and is also expensive. Therefore, it is important to prevent unauthorized copying of such software.

When an information word which belongs to the predetermined group appears in the flux of information words at the port of the memory it is recognized by the recognition means which thereupon generates a command signal.

In the described system the information words belonging to said predetermined group are information words which have a link to a further program word, which has to be addressed by the program counter during the subsequent program step by the execution of the program. If the program is not normally executed, i.e. for example when the program is copied, that further program word will not be addressed. Thereupon the command signal is confirmed and the first modification means are activated for applying a first modification operation which consists of replacing the program word addressed during said subsequent program step by a nuissance word, which is unrelated to said program word. The nuissance word is outputted at the first date output of the memory unit. The consequent thereof is that the copied program has become useless because it contains at least one nuissance word which disturbs the execution of the program.

The present invention be distinguished from the described system by that the first modification operation is differently implemented.

A data processing system according to the present invention is characterized in that said first modification operation being applied on the address part of said program word upon which the command signal was generated, said protection unit further comprises second modification means, having a fourth input connected to said first address input and a second address output connected with said port, said second modification means being provided for applying a second modification operation upon a received address signal in order to compensate for the first modification operation.

The advantage of that data processing system is that there is always some difference between the flux of information words at the port of the memory and the flux of data- and address signals between the memory unit and the data processor notwithstanding that the program is copied or not. During a normal execution of the program, *i.e.* when the program is executed under control of the data processor and the instructions are executed according to the content of the program words, the second modification means will apply a second modification operation upon a received address signal. The second modification operation will compensate for the first modification operation so that the correct address word will be supplied to the port of the memory. The normal execution will thus not be perturbed. However when the program is copied, the modified program word, outputted at the first data output of the memory unit, will be included in the copied program, making the copied program useless.

A preferred embodiment of the data processing system according to the invention is characterized in that, each of said program words of said predetermined group comprises an instruction which acts on an equal-step progression of the program counter. Instructions which act on an equal-step progression of the program counter are instructions which causes the program counter to increment (or decrement) with more than one unit step, such as for example JUMP or GO-TO instructions. Those instructions have an address part which comprises information about the address of the subsequent program word to be addressed during the normal execution of the program. A modification of that address part applied by the first modification operation can efficiently disturb a copied program.

A further preferred embodiment of a data processing system according to the invention is characte-

rized in that the program words of said predetermined group comprise an opcode part, said recognition means comprise an opcode decoder for decoding the opcode part of the program words.

Another preferred embodiment of a data processing system according to the invention is characterized in that said recognition means comprise an address decoder for decoding the address words which belong to said predetermined group.

Simple implementations of the recognition means are thus obtained.

It is favourable that said first and said second modification operation comprises the application of a mathematical operation. The address part of a program word is generally composed of a number of binary bits. Mathematical operations are easily applied thereon.

It is favourable that said first modification means comprise an adder for adding a value to said address part, and that said second modification means comprise a substracting circuit for substracting said value from said address signal.

This offers an easy and fast realization of the first and the second modification operation.

It is favourable that said first modification means comprise a random generator for generating said value, said random generator having an output connected with said second modification means for supplying said value.

When said value is generated by a random generator it will be very difficult for an unauthorized copier to know which value was added to the address part, because each time a different value can be generated.

The invention will now be described in detail with reference to the accompanying drawing in which the sole Figure represents a simplified block diagram of a preferred embodiment of a data processing system according to the invention.

The data processing system illustrated in the Figure comprises a memory unit 10 and a data processor 14 for example a micro processor. The memory unit comprises a memory 12, for example a ROM or a PROM, and a protection unit 24. The data processor and the memory unit are connected to each other by means of an address bus 11 and a data bus 13. The memory and the protection unit are connected to each other by means of an internal bus 23. The protection unit comprises recognition means 16 which have a first input connected to the internal bus. The protection unit also comprises first modification means 17 which have a second input connected to the internal bus 23 and a first data output connected to the data bus 13, and second modification means 15 which have an address input connected to the address bus 11 and an address output connected to the internal bus 23.

The memory 12 is used for the storage of at least one program which can be executed by the data processor. The program(s) comprises a plurality of program words. Each program word is generally composed of a number of binary bits. Each program word is stored at a respective memory location having his respective address. A port of the memory is connected to the internal bus for supplying address words to the memory in order to fetch the respective program words which belong to that address word.

As suggested by his denomination the protection unit 24 serves to protect the program words, especially against illegal coyping. Therefore the protection unit provides that for a number of program words outputted at the terminal of the memory, a modification operation is applied thereon.

Several implementations are possible for the protection unit. The operation of the data processing system will now be described with reference to a preferred embodiment for the protection unit. In this preferred embodiment of the protection unit, the recognition means 16 comprise a jump instruction decoder 18 and a random number generator 19. The first modification means 17 comprise an adder 25 and the second modification means 15 comprise a substracting circuit 26. The random number generator has an output connected via a line 20 to an input of the adder and to an input of the substracting circuit.

Among the program words stored in the memory there are the well known jump instructions which act on the equal-step progression of the program counter. These jump instructions are recognizable by their characteristic opcode (operational code) part. The jump instruction decoder 18, which is an opcode decoder, decodes the opcode parts of the program words outputted at the port of the memory and supplied to the internal bus 23. When a jump instruction is decoded, the jump instruction decoder generates a command signal which is supplied via line 21 to the random number generator 19, to the adder 25, even as to the subtracting circuit 26. Thereupon the random number generator 19 generates a random number which is supplied via line 20 to the adder and the substracting circuit. The adder, which is connected to the internal bus 23, has also received the program word which comprises the jump instruction. Under control of the command signal the adder will add the random number to the address part (indicating the address to which to jump) of that jump instruction and produces a pseudo-jump address.

The modified program word with the pseudo-jump address is now transmitted via the data bus 13 to the data processor 14. Thereupon the program counter will indicate the program word at that pseudo-address. When the data processor 14 thereafter addresses, via the address bus 11, the memory unit to acquire the program word at the pseudo-address, this address is transmitted to the subtracting circuit 26 of the second modification means. After reception of the pseudo-address, the subtracting circuit substracts the random number from the pseudo-address and transmits the thus obtained original address to the memory. The jump instruction is thus correctly executed.

Each subsequent program word outputted from the memory 12 which is not a jump instruction is transmitted through the adder 25 onto data bus 13 without alteration. Since the program counter of the data processor, however, has been stepped forward to the pseudo-address, the second modification means 15 retains the random number for subtraction from each of the addresses placed on address bus 11 by the data processor before transmission to the memory.

This continues until another jump instruction is provided on the port of the memory 12. When that occurs jump instruction decoder 18 again causes the

random number generator 19 to operate to place another random number in adder 25 and subtracting circuit 26. The adder 25 operates as previously to place a pseudo-jump address on the data bus 13. The second modification means 15 substitutes the new random number for the old random number in order to address the memory 12 properly when the data processor transmits the pseudo-jump address to the memory unit 10. In this way a predetermined group of information words in the form of jump instructions stored in some of the memory locations of the memory 12 cause the first modification means 17 to change those jump addresses before transmission on the data bus 13.

Suppose now that the program words stored in the memory 12 are copied. The pseudo-addresses supplied on data bus 13 will than be incorporated in the copied program, making that copied program useless, because a wrong location in the program will be addressed if the copied program is executed. Further if the copier addresses the memory unit after the output of the pseudo-address, the supplied address will be modified by the second modification means. The copier will thus not know which location of the memory has been addressed. The copied program is thus totally useless.

In one form of the invention each jump instruction transmitted from the memory would contain a binary 1 in one bit location. In all other memory locations of the memory that bit location would contain a binary 0. In that embodiment the jump instruction decoder would take the form of a circuit which would respond to the binary 1 in the prescribed bit location and would consequently cause the generation of the command signal as previously described.

In an alternative form, all jump instructions would be located in a particular section of the memory and the recognition means 16 would comprise a comparator which would respond to the addresses in the locations in that section and cause the random number generator 19 to operate as previously described. The comparator is then for example connected to a storage element where said addresses are stored as indentifier information in order to enable the comparison. When all jump instructions are located in a particular section of the memory 12, then the recognition means could for example comprise an address decoder for decoding the addresses of that particular section. Other types of recognition means are also known to those skilled in the art and could be substituted for those disclosed.

The recognition means could also react on other instructions than only the jump instructions, such as for example GO-TO instructions or any other instructions which act on an equal step progression of the program counter.

Several implementations are also possible for the first and the second modification means, which could for example comprise an inverter, for inverting one of more bit locations in the address part of the jump instruction. For this implementation a random number generator is of course redundant.

In an alternative embodiment the first modification means would for example comprise a first address table, addressed by the address part of the jump instruction and comprising for each jump instruction a substitution address. The second modification means would then of course comprise a second address table, provided for restoring the original address part.

It is understood that various modifications to the above described system of the invention will become apparent to those skilled in the art and that the arrangement described herein is for illustrative purposes and is not to be considered restrictive.

CLAIMS

1. Data processing system comprising a data processor and a memory unit which comprises a protection unit and a memory for the storage of at least one program comprising a plurality of program words, said memory having a port for the exchange of information words, each information word comprises a program word and his respective address word, said protection unit comprises:

– recognition means having a first input connected to said port and being provided for recognizing out of the flux of information words at said port those which belong to a predetermined group wherein the information words have a program word which comprises an address part for addressing a further program word, said recognition means being further provided for generating a command signal thereupon;

– first modification means, having a second input connected to said port and a third input connected to said recognition means for receiving said command signal, said first modification means being provided for applying under control of said command signal a first modification operation on a received program word, said first modification means being connected to a first data output of said memory unit;

said data processor comprises:

– a data input connected to said first data output for receiving data signals

– a program counter which is settable under control of received data signals;

– a first address output connected to a first address input of the memory unit for supplying address signals in a sequence determined by said program counter;

characterized in that, said first modification operation being applied on the address part of said program word upon which the command signal was generated, said protection unit further comprises second modification means, having a fourth input connected to said first address input and a second address output connected with said port, said second modification means being provided for applying a second modification operation upon a received address signal in order to compensate for the first modification operation.

2. A data processing system as claimed in Claim 1, characterized in that each of said program words of said predetermined group comprises an instruction which acts on an equal-step progression of the program counter.

3. A data processing system as claimed in Claim 1 or 2, characterized in that the program words of said predetermined group comprise an opcode part, said recognition means comprise an opcode decoder for decoding the opcode part of the program words.

4. A data processing system as claimed in Claim 1 or 2, characterized in that said recognition means comprise an address decoder for decoding the address words which belong to said predetermined group.

5. A data processing system as claimed in Claim 1 or 2, characterized in that said recognition means comprise a storage element for storing an identifier information for each of the information words of said predetermined group, and a comparator having a first comparator input connected to said storage element and a second comparator input connected with said first input for realizing said recognition by comparing the identifier information with the supplied information words, said command signal being generated upon correspondence between said identifier information and said information word.

6. A data processing system as claimed in one of the Claims 2, 3, 4 or 5, characterized in that each program word of said predetermined group comprises a jump instruction and the address word of the program word to which jump.

7. A data processing system as claimed in Claim 5, characterized in that said indentifier information comprises at least a part of the content of the program word.

8. A data processing system as claimed in Claim 5, characterized in that said identifier information comprises at least a part of the content of the address word.

9. A data processing system as claimed in one of the preceding Claims, characterized in that said first and said second modification operation comprises the application of the mathematical operation.

10. A data processing system as claimed in Claim 9, characterized in that, said first modification means comprise an adder for adding a value to said address part, and that said second modification means comprise a subtracting circuit for subtracting said value from said address signal.

11. A data processing system as claimed in Claim 10, characterized in that said first modification means comprise a random generator for generating said value, said random generator having an output connected with said second modification means for supplying said value.

12. A memory unit for use in a data processing system as claimed in any of the preceding claims, characterized in that said memory unit comprises a memory and a protection unit.

13. Protection means to be used in a data processing system as claimed in any of the claims 1 to 11.

14. A memory unit as claimed in Claim 12, characterized in that the memory unit is constructed using an integrated circuit technique, and that the memory and the protection unit are integrated on the same chip surface.

15. A video game module comprising a memory unit as claimed in Claim 12 or 14.

16. A data processing system substantially as hereinbefore described with reference to the accompanying drawing.

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